Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FREDERIC BOUTAND, JASON JONES, MARC COUVRAT, OLIVER MOUGENOT and MANSOOR A. CHISHTIE

Appeal No. 1999-0153
Application No. 08/488,394

ON BRIEF

Before RUGGIERO, LALL, and DIXON, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claim 1, the sole claim in the application.

The claimed invention relates to a test circuit for controlling the testing of a circuit having portions which use

either a synchronous clock signal or an asynchronous clock signal. The test circuitry includes two multiplexers for selecting between test signal clocks and normal function clocks. For the portion of the circuit to be tested that uses internal or synchronous signals, the first multiplexer selects between the normal internal functional clock and a test clock. For the portion of the tested circuit that utilizes external or asynchronous clock signals, the second multiplexer selects between the external clock and the output of the first multiplexer. Appellants assert at page 81 of the specification that the described arrangement allows the internal clock signal or a test clock signal to be supplied to all portions of a circuit to be tested regardless of whether the circuit is normally clocked by synchronous or asynchronous signals.

Claim 1 is illustrative of the invention and reads as follows:

1. A test circuit for controlling the testing of a circuit having portions using either synchronous or asynchronous clock signals, comprising:

a first multiplexer for selectively providing as an output either said synchronous clock signal or a test clock

signal to said portion of said circuit using said synchronous clock signal, and

a second multiplexer for selectively providing said output from said first multiplexer or said asynchronous clock signal to said portion of said circuit using said asynchronous clock signal.

The Examiner relies on the following prior art:

Staiger 4,203,543 May 20, 1980

Claim 1 stands finally rejected under 35 U.S.C. § 103 as being unpatentable over Staiger.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the

rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention set forth in claim 1. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-

Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert.denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Appellant's response to the Examiner's obviousness rejection of claim 1 asserts the Examiner's failure to establish a prima facie case of obviousness since all of the claim limitations are not suggested or taught by the Stagier reference. Initially, Appellants contend (Brief, page 4) that the Examiner has provided no support for the conclusion that the input of synchronous and asynchronous clock signals as presently claimed to the multiplexers in Staiger rather than selected delay times would be a matter of design choice.

After reviewing the Staiger reference in light of the arguments of record, we are in agreement with Appellants' position as stated in the Brief. In our view, the Examiner's reliance on design considerations as a basis for the proposed modification of Staiger is not well founded. Appellants' disclosed intended function of applying synchronous internal clocking signals or test clocking signals to various portions of a circuit to be tested can only be achieved through the circuit arrangement recited in appealed claim 1 which requires synchronous and asynchronous clocking inputs to the two claimed multiplexers. In our opinion, the Examiner's finding of the particular claimed multiplexer inputs to be merely a design consideration is totally devoid of any support on the record.

We also find persuasive Appellants' further argument (Brief, page 5) that the Examiner has unreasonably interpreted the language of appealed claim 1 as requiring multiplexer outputs to only a single circuit portion (an arrangement disclosed by Staiger) rather than a plurality of circuit portions. In the Examiner's analysis (Answer, pages 4 and 5)

the language "...a circuit having portions using either synchronous or asynchronous clock signals" appearing in the preamble of claim 1 is broadly interpreted as meaning that all portions of a circuit can use either synchronous or asynchronous signals. Under this interpretation, the Examiner asserts that the output of the multiplexer circuits can be to a single circuit portion (as in Staiger), which single circuit portion can use either synchronous or asynchronous signals.

We can find no basis on the record for the Examiner interpreting the claim language in this manner. It is apparent to us that, when the language of the claim preamble is read in conjunction with the language in the body of the claim, the outputs of Appellants' multiplexers are recited as being applied to different portions of the tested circuit, a concept not taught or suggested in Staiger. It is also apparent from the Examiner's line of reasoning in the Answer that, since the Examiner has mistakenly interpreted the disclosure of Staiger as disclosing the particular claimed multiplexer outputs, the obviousness of this feature has not

been addressed. We would further point out that appealed claim 1 also requires the selection by the first multiplexer of an input synchronous clock signal or a test clock signal, a disclosure of which we find lacking in Staiger.

Since all of the claim limitations are not taught or suggested by the applied prior art, it is our opinion that the Examiner has not established a prima facie case of obviousness with respect to appealed claim 1. Accordingly, we do not sustain

the Examiner's 35 U.S.C. § 103 rejection of claim 1 and,

therefore, the Examiner's decision rejecting claim 1 is reversed.

REVERSED

JOSEPH F. RUGGIERO Administrative Patent Judge	)	
PARSHOTAM S. LALL Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH L. DIXON Administrative Patent Judge	)	

JR/RWK

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